REMARKS/ARGUMENTS

Applicants thank the Examiner for his careful review of this application. Claims 4, 5, and 6 have been amended. Claims 1-7 remain pending. Applicants respectfully request reconsideration of the application in view of the above amendment and the following remarks submitted in support thereof.

Rejections under 35 U.S.C. §102:

The Examiner rejected claims 4-6 under 35 U.S.C. §102(b), as being anticipated by Oberman et al. (US Pat. 6,298,367). The rejection is respectfully traversed. The teachings of Oberman et al. do not show the currently claimed invention of independent claims 4-6. Independent claim 4 defines a machine readable medium containing data structure having an instruction therein for determining which values from a local storage containing floating point values to send to a floating point execution unit, in parallel to a compare unit. In the claimed invention, the rounding choice is calculated in parallel with the adder unit performing the subtraction. This enables the adder unit to have the correct rounding choice available at the instant the adder unit completes the subtraction.

Parallelism is accomplished by having a correct rounding choice calculated using an end-around-carry (EAC) value while the adder unit completes the subtraction. In the claimed invention, the EAC bit is calculated and provided using the output from the compare unit. Whereas, in Oberman, the right shifter 314A and right shifter 314 b provides the values to GRS logic 320 and the selection unit 350 uses these values to calculate selection values for all possible scenarios. The right shifter 314a and 314b are similar to the mantissa alignment in the claimed invention. This implies that the invention in Oberman is not accomplishing parallelism as in the claimed invention. The selection unit 350 in Oberman receives the

output from the adder unit and conveys a signal to the multiplexer shift unit 360. This shows that the selection unit calculates the rounding choice subsequent to the adder unit completes the subtraction. Thus, the selection unit 350 is incapable of providing a rounding choice to the adder unit at the instant the adder unit completes the subtraction.

Moreover, the Examiner asserts the compare unit of the claimed invention and the combination of exponent comparator unit 308, multiplexer inverter unit 330, and adder unit 340 of Oberman to be the same. Firstly, the output from the exponent comp 308 i.e. the largest input exponent 309 is provided only to the exponent adjust component 370. The output 309 is not utilized anywhere in the rounding choice process as indicated by the Examiner. Additionally, the comparator in Oberman does not function like the one in the claimed invention where the comparators make available an output that may be used to calculate the EAC bit value which is used to make a selection between the sum and the sum + 1. In fact, Oberman does not provide any element that is similar to the comparator of the claimed invention. Moreover, if the adder unit 340 were part of the comparator, then the addition and the rounding choice could not be done in parallel as recited in the claimed invention.

It is emphasized that Oberman et al. does not teach a parallel method (as claimed). This teaching is evident from Figures 5, 6 and 9. Accordingly, the Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102(b) rejection of claims 4-6.

To establish a *prima facie* case of obviousness, the prior art reference must teach or suggest all the claim limitations (see MPEP2143). As can be seen from above, Oberman et al. does not teach all the features of the claimed invention.

Independent claim 5 was rejected under 35 U.S.C. §102(b), as being anticipated by Oberman et al. Applicants respectfully traverse the rejection. As described above, in

Oberman the EAC bit value is not computed in parallel with the adder unit. The EAC bit value in Oberman is calculated as part of the addition process. Also, Oberman does not have a compare unit that works in parallel with the adder unit as taught in the claimed invention. Therefore, Applicants respectfully request the Examiner to withdraw the 35 U.S.C. §102(b) rejection of claim 5.

Similarly, independent claim 6 includes the comparator unit which works in parallel with the adder unit to make available an output that is used to calculate the EAC bit value. The EAC value calculation is done independent of the addition steps carried out by the adder unit. Accordingly, Applicants submit that the independent claim 6 is patentable under 35 U.S.C. §102(b) for the reasons set forth above.

Allowable Subject Matter

Claims 1-3 and 7 are allowed.

Conclusion

In view of the foregoing, the Applicants respectfully submit that all the pending claims 4,5, and 6 are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is requested to contact the undersigned at (408) 774-6926. If any additional fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP285). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,

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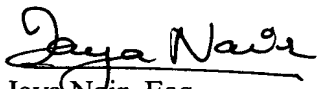

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